REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1, 5-7, 8, 11, 12, 14-16, 20-23, 26, 27, 29, and 30 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669); claims 2, 9, 17, and 24 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) and in further view of Barker (U.S. Patent No. 3,609,504); and claims 3, 4, 10, 13, 18. 19, 25 and 28 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) in further view of Patel (U.S. Patent No. 5,018,148). These rejections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1 - 30.

2. Claims 1, 5-7, 8, 11, 12, 14-16, 20-23, 26, 27, 29, and 30 have been rejected under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669). The applicant respectfully disagrees with the Examiner's characterization of the present claims in view of the prior art cited.

In particular, Urbano does not teach efficient use of a battery in a handheld device to initiate one of a plurality of fail safe algorithms based on when one or more of the overload condition, the system low voltage condition, and the battery low voltage condition are detected. Urbano, however, does teach an ultrasound system that includes techniques to reduce power consumption. For

instance, Urbano teaches that power consumption by electrical components is reduced in one or both of the ultrasound data path and the ultrasound processing control. (column 3, lines 12 - 15) Urbano further teaches, at column 5, lines 1 - 9 that:

> In one embodiment for reducing power consumption, one or more electrical components in one or more of the subsystems of the ultrasound system **10** operate in a reduced power mode. During use, the electrical component operates in a full power mode or an increased power state. During a non-use period, the electrical component may be controlled to operate in a low power mode or a decreased power state. For example, a digital electrical component is placed into a sleep state for low power consumption.

Urbano further teaches that, during the non-use periods, the low power mode or decreased power state may achieved in a variety of ways. For example, at column 5, lines 47 - 50, Urbano discloses at reduced clock rate:

> When the electrical component **40** is not being used, the control **44** controls the output of the clock to halt or reduce the toggling rate, reducing consumption of power by the electrical component **40**.

At column 5, lines 62 - 66, Urbano discloses a standby mode or suspend mode:

> instruction or external signal. In these embodiments, the control path comprises a controller for generating the external suspend or standby signal. Alternatively, the electrical component includes a time-based or other internal instruction for automatically entering a suspend or standby mode during periods of nonusage. As an alternative or in addition

At column 6, lines 5 - 21, Urbano discloses a return to initialization state:

> electrical components. For example, a field programmable gate array, such as a random access memory based field programmable gate array, has an initial unprogrammed state for receiving instructions and then operates in a programmed state during the processing of data using the programmed instructions. Power consumption is less in the initial unprogrammed state. To enter a low-power mode or decreased power state, the field programmable gate array is placed into the unprogrammed state. For example, an Altera Flex 10 K field programmable gate array device is forced into an unprogrammed state by asserting a "configuration" input without loading any programming data. For processing and operating in a full power mode, program data is loaded into the field programmable gate array. Other devices that use less power during an initialization stage or other state may be operated in a similar manner for decreased power consumption. Additionally or alternatively, a clock frequency asso-

At column 6, lines 28 - 31, Urbano discloses a reduced power supply state:

> low power mode or decreased power state. For example, a voltage supplied to an analog component, such as an analog amplifier, is reduced. A voltage regulator may include a control for reducing the output voltage. As another example,

Urbano further teaches that the various lower power states may be initiated in a variety of ways. For example, Urbano discloses that a user activated button (column 7, lines 4 - 6), expiration of an inactivity time out period (column 7, lines 14 - 17), expiration of a wait to receive input time period (column 7, lines 20 - 22), and a user configuration (column 7, lines 33 - 36).

Accordingly, Urbano teaches an ultrasound system that has power reduction techniques to place un-used components into low power states that may be initiated in variety of ways. Urbano does not teach or suggest sensing for one or more of low battery, overload, or system low voltage and initiating a fail safe algorithm in response thereto.

Choudhury teaches a digital signal processor controlled uninterruptible power supply (UPS), where the basic architecture of the UPS is shown in Figure 2 and the DSP of Figure 3 produces the pulse width modulated (PWM) control signals for transistors 211, 213, 241, 251, 231, and 233 of Figure 2. The UPS has two modes of operation: a normal mode and a battery back up mode. In the normal mode, the UPS produces an AC output and charges the battery. In the battery back up mode, the UPS converts the battery voltage to a DC bus voltage and, via a DC-AC inverter, produces the AC output from the DC bus voltage. (column 3, lines 28 - 44)

Choudhury teaches that the DSP produces the PWM control signals PWM1 - PWM6 (column 4, lines 45 - 49) by performing the functions of Figures 5 - 13. In Figure 10 and the corresponding text at column 8, lines 22 - 57, the DSP produces PWM5 and PWM6 signals for transistors 231 and 233 such that the DC/AC inverter portion of the UPS is regulated. The PWM5 and PWM6 signals are produced by comparing a digitized output voltage (Vout) with a reference sinusoid waveform (Vref) to produce a difference. The difference is processed by a compensator (P11) to produce a reference current for an inner current loop. In addition, a digitized inductor current feedback (Iout) is compared with the output of the first compensator (P11) to produce a second difference. A second compensator (P12) produces PWM5 and PWM6 signals from the second difference.

In Figure 11 and the corresponding text of column 8, line 58, through column 9, line 25, Choudhury teaches that the DSP generates a PWM3 signal and disable a PWM4 signal

for charging the 110 volt DC battery 105 from the 400 volt DC bus. In this mode, the DSP senses the battery current (Ib), the battery voltage (Vb), and V- with respect to ground. The battery voltage and battery current are used to determine which of the three battery charge modes (e.g., trickle, bulk charge, and over charge) to initiate.

In Figure 12 and the corresponding text of column 9, line 26, through column 10, line 11, Choudhury teaches that the DSP generates PWM1 and PWM2 signals to regulate the DC bus to 400 volts DC. To do this, the DSP senses the AC input voltage (Vs), the AC input current (Is), and the DC bus voltage (V-, V+). Based on these inputs, the pulse width of PWM1 and PWM2 signals is determined such that the DC bus is regulated to 400 volts.

In Figure 13 and the corresponding text of column 10, lines 12 - 35, Choudhury teaches that the DSP generates PWM4 signal and disables PWM3 signal to produce a boost converter for the battery back up mode. In this mode, the DSP senses the battery current (Ib), the battery voltage (Vb), and V- with respect to ground to establish the pulse width of the PWM4 signal.

From the above passages, Choudhury teaches a UPS that has a DSP producing the control signals for the normal mode and the battery back up mode of the UPS. Choudhury does not teach of suggest sensing for one or more of low battery, overload, or system low voltage and initiating a fail safe algorithm in response thereto.

Since each of the independent claims 1, 8, 12, 16, 23, and 27 of the present patent application includes a limitation for sensing at least one of a low battery condition, an overload condition, or a system low voltage condition and initiating a fail safe algorithm in response thereto, the applicant believes that the combination of Urbano with Choudhury fails to render the present claims obvious. In particular, the power reduction techniques of Urbano in combination with the normal and battery back up modes of generating PWM signals of Choudhury do not suggest a method and apparatus for initiating a fail safe algorithm in response to sensing a low battery condition, an overload condition, and/or a low system supply voltage condition.

3. Claims 2, 9, 17, and 24 have been rejected under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) and in further view of Barker (U.S. Patent No. 3,609,504). The applicant respectfully disagrees.

As demonstrated above, the combination of Urbano and Choudhury fail to render the independent claims of the present patent application obvious. Thus, the applicant believes that the present claims are not obvious in view of the cited prior art.

4. Claims 3, 4, 10, 13, 18. 19, 25 and 28 have been rejected under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) in further view of Patel (U.S. Patent No. 5,018,148).

As demonstrated above, the combination of Urbano and Choudhury fail to render the independent claims of the present patent application obvious. Thus, the applicant believes that the present claims are not obvious in view of the cited prior art.

For the foregoing reasons, the applicant believes that claims 1 - 30 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

By: /Timothy W. Markison reg. 33,534/
Timothy W. Markison
Phone: (512) 342-0612
Fax No. (512) 342-1674

CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Alexandria, Virginia 22313, on the date below:

6-16-05
Date

Diane Hudson
Signature